IN THE CLAIMS

Please amend the claims as follows:

1-30. (Cancelled)

31. (Previously Presented) A system comprising:

a random access memory to store at least a part of a number of processor instructions; and

a processor to have a number of microarchitectural states during execution of the number of processor instructions, the processor comprising:

a main pipeline to execute the number of processor instructions;

a conjugate mapping table to store at least one entry that includes a trigger and an associated target related to execution of the number of processor instructions; and

an h-flow pipeline to execute h-flow code related to the associated target if the trigger is satisfied during execution of the number of processor instructions, wherein the h-flow pipeline is to modify one of the number of microarchitectural states based on execution of the h-flow code.

32. (Previously Presented) The system of claim 31, wherein the processor further comprises a dynamic code analysis block to generate the h-flow code based on an analysis of the execution of the number of processor instructions by the main pipeline.

33. (Previously Presented) The system of claim 31, wherein the processor further comprises a microarchitectural structure to store the number of microarchitectural states.

34. (Previously Presented) The system of claim 31, wherein the number of microarchitectural states include values stored in register banks, branch target buffers or data cache.

35. (New) A method comprising:

executing a number of processor instructions;

storing, in a conjugate mapping table, at least one entry that includes a trigger and an associated target related to the execution of the number of processor instructions; and

executing, in an h-flow pipeline, h-flow code related to the associated target if the trigger is satisfied during the execution of the number of processor instructions, wherein the h-flow pipeline is to modify one of the number of microarchitectural states based on execution of the h-flow code.

36. (New) The method of claim 35 further comprising:

generating the h-flow code based on an analysis of the execution of the number of processor instructions by the main pipeline.

37. (New) The method of claim 35 further comprising:

storing the number of microarchitectural states.

38. (New) The method of claim 35, wherein the number of microarchitectural states include values stored in register banks, branch target buffers or data cache.

39. (New) The method of claim 35, wherein the trigger is selected from a group consisting of instruction triggers, data triggers, state triggers and event triggers.

40. (New) The method of claim 35, wherein the trigger can include single atomic attributes or can include vector triggers.

41. (New) A computer-readable medium containing computer instructions which when executed will perform the following:

executing a number of processor instructions;

storing, in a conjugate mapping table, at least one entry that includes a trigger and an associated target related to the execution of the number of processor instructions; and

executing, in an h-flow pipeline, h-flow code related to the associated target if the trigger is satisfied during the execution of the number of processor instructions, wherein the h-flow pipeline is to modify one of the number of microarchitectural states based on execution of the h-flow code.

42. (New) The computer-readable medium of claim 0 further containing computer instructions which when executed will perform:

generating the h-flow code based on an analysis of the execution of the number of processor instructions by the main pipeline.

43. (New) The computer-readable medium of claim 0 futher containing computer instructions which when executed will perform:

storing the number of microarchitectural states.

44. (New) The computer-readable medium of claim 0, wherein the number of microarchitectural states include values stored in register banks, branch target buffers or data cache.

45. (New) The computer-readable medium of claim 0, wherein the trigger is selected from a group consisting of instruction triggers, data triggers, state triggers and event triggers.

46. (New) The computer-readable medium of claim 0, wherein the trigger can include single atomic attributes or can include vector triggers.